CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of producing an imaging device, comprising:

forming a photosensitive region;

forming a diffusion region;

forming a gate structure;

forming an insulating layer over the photosensitive region, the gate structure and the diffusion region; and

removing a first portion of the insulating layer over the diffusion region, leaving a spacer at a side of the gate structure and leaving a second portion of the insulating layer over the photosensitive region.

2. The method of claim 1, wherein the imaging device is a CMOS imager.

3. The method of claim 2, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

4. The method of claim 2, wherein the CMOS imager comprises at least one of a transfer gate, reset gate, row select gate, storage gate, dual conversion gate, and high dynamic range gate.

5. The method of claim 1, wherein the imaging device has periphery circuits.

6. The method of claim 1, wherein the imaging device is a CCD imager.

7. The method of claim 1, wherein the diffusion region is selected from the group consisting of a floating diffusion, N^+ active area, P^+ active area, N^- active area, P^- active area, and storage node diffusion.

8. The method of claim 7, wherein the first portion of the insulating layer is removed from over at least one of the floating diffusion, N^+ active area, P^+ active area, N^- active area, P^- active area, and storage node diffusion.

9. The method of claim 1, wherein the photosensitive region is selected from the group consisting of a photodiode, photogate, and photoconductor.

10. The method of claim 9, wherein the photodiode is a p-n-p photodiode.

11. The method of claim 1, wherein the insulating layer is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

12. The method of claim 1, further comprising implanting dopant with the spacer as a mask.

13. The method of claim 1, wherein the spacer is left on at least one side of at least one gate structure.

14. The method of claim 1, wherein the spacer is left on both sides of at least one gate structure.

15. The method of claim 1, wherein the gate structure comprises a gate oxide and a gate conductor.

16. The method of claim 15, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

17. The method of claim 15, wherein the gate structure comprises a second insulator over the gate conductor.

18. The method of claim 17, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

19. The method of claim 1, wherein the gate structure is an n-channel gate.

20. The method of claim 1, wherein the spacer is formed by a masked spacer etch.

21. The method of claim 12, wherein the mask used to define the masked spacer etch remains during the dopant implantation.

22. The method of claim 1, wherein the insulating layer has a thickness within the range of about 100 to about 1500 Angstroms.

23. The method of claim 22, wherein the insulating layer has a thickness within the range of about 200 to about 1000 Angstroms.

24. The method of claim 12, wherein the dopant is an n-type dopant.

25. A method of producing an imaging device, comprising:

forming an array of photosensitive regions;

forming first and second sets of gate structures, the first set of gate structures being formed in said array and the second set of gate structures being formed in a periphery outside said array;

forming first and second sets of diffusion regions;

forming an insulating layer over the photosensitive region, the gate structures and the diffusion regions in the array and the periphery;

removing a first portion of the insulating layer over the first set of diffusion regions in the array, leaving a spacer at at least one side of at least one gate structure

of the first set of gate structures in the array and leaving a second portion of the insulating layer over the photosensitive regions; and

removing a third portion of the insulating layer over the second set of diffusion regions in the periphery, leaving a spacer at at least one side of at least one gate structure of the second set of gate structures in the periphery.

26. The method of claim 25, wherein the gate structure of each said first and second sets of gate structures comprises a gate oxide and a gate conductor.

27. The method of claim 26, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

28. The method of claim 26, wherein the gate structure comprises a second insulator over the gate conductor.

29. The method of claim 28, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

30. The method of claim 25, wherein each spacer is formed by a masked spacer etch.

31. The method of claim 25, further comprising implanting dopant with each spacer as a mask.

32. The method of claim 31, wherein the mask used to define the masked spacer etch remains during the dopant implantation.

33. The method of claim 25, wherein the insulating layer has a thickness within the range of about 100 to about 1500 Angstroms.

34. The method of claim 33, wherein the insulating layer has a thickness within the range of about 200 to about 1000 Angstroms.

35. The method of claim 31, wherein the dopant is an n-type dopant.

36. The method of claim 25, wherein the gate structures are comprised of at least one of an n-channel gate and a p-channel gate.

37. The method of claim 25, wherein the imaging device is a CMOS imager.

38. The method of claim 37, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

39. The method of claim 37, wherein the CMOS imager comprises at least one of a transfer gate, reset gate, row select gate, storage gate, dual conversion gate, and high dynamic range gate.

40. The method of claim 25, wherein the imaging device is a CCD imager.

41. The method of claim 25, wherein the insulating layer is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

42. The method of claim 25, wherein each of the first and second sets of diffusion regions is selected from the group consisting of a floating diffusion, N^+ active area, P^+ active area, N^- active area, P^- active area, and storage node diffusion.

43. The method of claim 42, wherein the first portion of the insulating layer is removed from over at least one of the floating diffusion, N^+ active area, P^+ active area, N^- active area, P^- active area, and storage node diffusion.

44. The method of claim 25, wherein the first and third portions of the insulating layer are removed by spacer etching.

45. The method of claim 25, wherein the first and third portions of the insulating layer are removed by at least one of an anisotropic dry etch and an isotropic etch.

46. The method of claim 25, wherein the imaging device has periphery circuits.

47. The method of claim 25, further comprising implanting dopant with each spacer as a mask.

48. The method of claim 25, wherein each spacer is left on at least one side of at least one gate structure.

49. The method of claim 25, wherein each spacer is left on both sides of at least one gate structure.

50. The method of claim 25, wherein each of the photosensitive regions is selected from the group consisting of a photodiode, photogate, and photoconductor.

51. The method of claim 50, wherein the photodiode is a p-n-p photodiode.

52. A method of producing an imaging device, comprising:

forming photosensors and gate structures for N-channel transistors within a pixel array, and forming gate structures for N-channel and P-channel transistors outside said pixel array;

forming a spacer material over said photosensors and gate structures;

forming a first mask layer that covers said photosensors and gate structures for P-channel transistors and does not cover at least one of said gate structures for N-channel transistors;

etching said spacer material to form at least one sidewall spacer on at least one said gate structure for an N-channel transistor, wherein said photosensors remain covered with said spacer material and said first mask layer;

implanting dopant to form N type source/drain regions for at least one N-channel transistor;

forming a second mask layer that covers said photosensors and gate structures for N-channel transistors and does not cover at least one of said gate structures for P-channel transistors;

etching said spacer material to form at least one sidewall spacer on at least one gate structure for a P-channel transistor, wherein said photosensors remain covered with said spacer material; and

implanting dopant to form P type source/drain regions for at least one P-channel transistor.

53. The method of claim 52, wherein each of said gate structures comprises a gate oxide and a gate conductor.

54. The method of claim 53, wherein the gate conductor comprises at least one of a polysilicon, silicide, metal, or combination of a polysilicon, silicide, and metal.

55. The method of claim 53, wherein each of said gate structures comprises a second insulator over the gate conductor.

56. The method of claim 55, wherein the second insulator comprises at least one of an oxide, nitride, metal oxide, or combination of an oxide, nitride, and metal oxide.

57. The method of claim 52, wherein the spacer material has a thickness within the range of about 100 to about 1500 Angstroms.

58. The method of claim 57, wherein the spacer material has a thickness within the range of about 200 to about 1000 Angstroms.

59. The method of claim 52, wherein the imaging device is a CMOS imager.

60. The method of claim 59, wherein the CMOS imager comprises a three-transistor, four-transistor, five-transistor, six-transistor, or seven-transistor architecture.

61. The method of claim 52, wherein the spacer material is selected from the group consisting of an oxide, nitride, oxide/nitride, and metal oxide.

62. The method of claim 52, wherein each of the photosensors is selected from the group consisting of a photodiode, photogate, and photoconductor.

63. The method of claim 52, wherein implanting dopant to form N type source/drain regions comprises implanting with phosphorus, arsenic or antimony.

64. The method of claim 63, wherein said dopant is implanted at a dose of about 5×10^{14} atoms/cm^2 to about 5×10^{16} atoms/cm^2.

65. The method of claim 52, wherein implanting dopant to form P type source/drain regions comprises implanting with boron, boron-difluoride or indium.

66. The method of claim 65, wherein said dopant is implanted at a dose of about 5×10^{14} atoms/cm^2 to about 5×10^{16} atoms/cm^2.

67. An imaging array comprising:

row lines and column lines; and

for each combination of a row line and a column line, a pixel that includes:

a photosensitive region;

a diffusion region;

a gate structure;

a layer of an insulating material over the photosensitive region; and

a spacer of the insulating material at at least one side of the gate structure.

68. The imaging array of claim 67, wherein the pixel is part of a CMOS imager.

69. The imaging array of claim 67, wherein the pixel is part of a CCD imager.

70. An integrated circuit with an imaging array comprising:

row lines and column lines at a surface of a substrate;

for each combination of a row line and a column line, a pixel that includes:

a photosensitive region;

a diffusion region;

a gate structure;

a layer of an insulating material over the photosensitive region; and

a spacer of the insulating material at at least one side of the gate structure; and

a peripheral circuit, said peripheral circuit having at least one transistor with a gate structure and a spacer of the insulating material at at least one side of the gate structure.

71. The integrated circuit of claim 70, wherein the pixel is part of a CMOS imager.

72. The integrated circuit of claim 70, wherein the pixel is part of a CCD imager.

73. An imaging device comprising:

a semiconductor substrate; and

a pixel array, said pixel array comprising:

at least one photosensor, said photosensor covered by a spacer material;

a diffusion region;

at least one N-channel transistor, wherein at least one spacer formed from said spacer material is along at least one side of at least one of each said N-channel transistor's gate; and

at least one of an N-channel transistor or a P-channel transistor outside said pixel array, wherein spacers formed from said spacer material are along at least one side of at least one of either said P-channel or N-channel transistor's gate.

74. The imaging device of claim 73, further comprising a translucent or transparent insulating layer formed over said imaging device, said insulating layer selected from the group consisting of SiO_2, BPSU, TEOS, BPSG, PSG, BSG, and SOG.

75. The imaging device of claim 74, wherein electrical contacts are formed through said insulating layer.

76. An image pixel array in a CMOS imaging device, comprising:

at least one photosensor, said photosensor covered by a spacer material;

a diffusion region; and

at least one N-channel transistor having a gate and, along at least one side of the gate, a spacer formed of said spacer material.

77. The image pixel array of claim 76, wherein said photosensor is selected from the group consisting of a photodiode, photogate, photoconductor, and other photon to charge converting device for initial accumulation of photo-generated charge.

78. The image pixel array of claim 76, wherein said spacer material comprises at least one of an oxide, nitride, oxide/nitride, and metal oxide.

79. The image pixel array of claim 76, wherein said pixel array comprises about 0.1 megapixels to about 20 megapixels.

80. The image pixel array of claim 76, wherein each pixel of said pixel array comprises a pinned photodiode for performing photoelectric conversion.

81. An imager system, comprising:

a processor; and

an imaging device connected to provide signals to said processor, said imaging device comprising:

a semiconductor substrate; and

a pixel array, said pixel array comprising:

at least one photosensor, said photosensor covered by a spacer material;

a diffusion region;

at least one N-channel transistor, wherein at least one spacer formed from said spacer material is along at least one side of at least one of each said N-channel transistor's gate; and

at least one N-channel or P-channel transistor outside said pixel array,, wherein at least one spacer formed from said spacer material is along at least one side of at least one of each said N-channel and P-channel transistor's gate.

82. The imager system of claim 81, wherein said spacer material comprises at least one of an oxide, nitride, oxide/nitride, and metal oxide.

83. An imager system, comprising:

a processor; and

an integrated circuit connected to provide signals to said processor, said integrated circuit comprising:

row lines and column lines at a surface of a substrate;

for each combination of a row line and a column line, a pixel that includes:

a photosensitive region;

a diffusion region;

a gate structure;

a layer of an insulating material over the photosensitive region; and

a spacer of the insulating material at at least one side of at least one gate structure; and

a peripheral circuit, said peripheral circuit having at least one transistor with a gate structure having a spacer of the insulating material at at least one side of the gate structure.